

TWO MASK PHOTORESIST EXPOSURE PATTERN
FOR DENSE AND ISOLATED REGIONS

BACKGROUND OF THE INVENTION

5 [0001] The invention relates generally to semiconductor device manufacturing and, more particularly, to photolithographically forming plural features using different illumination conditions.

10 [0002] Semiconductor devices having smaller and smaller features are approaching a limit in which such features may be formed by conventional photolithography methods. For example, conventional photolithography methods produce vias in an insulating layer, as illustrated Figures 1A and 1B. A positive photoresist layer 3 is formed over an insulating layer 1 in which it is desired to form a first and second via. A plurality of regions 5A, 5B, 5C and 7 in the photoresist layer 3 are simultaneously exposed to actinic light 8 through openings 11A, 11B, 11C and 13 in a single mask or reticle 9, as illustrated in Figure 1A. The terms mask and reticle are used interchangeably, with the term reticle often applied to a mask used in step and repeat exposure systems. The exposed regions 5A, 5B, 5C and 7 are then developed and removed, while unexposed regions 6 remain as shown in Figure 1B. A gas or liquid etching medium is then supplied through the openings 5A, 5B, 5C and 7 in the photoresist layer 3 to etch vias 15A, 15B, 15C and 17 in layer 1, as illustrated in Figure 1C.

[0003] However, as the density of the vias has increased and the size of the vias has decreased, diffraction effects often result in patterning errors. These errors result in via size or location that deviate from the desired size or location.

25 [0004] Furthermore, only certain values of exposure dose and defocus are allowed to form an exposed region in the photoresist layer within the allowed design parameters. A set of allowed exposure dose and defocus values that may be used in exposing a particular region is referred to as a process window.

[0005] It has been suggested that the process window 101 for exposing dense regions in a photoresist layer differs from the process window 103 for exposing isolated regions in the photoresist layer, as shown in Figure 2A. See A. R. Newreueher and C. A. Mack, SPIE Short Course Note SC102, "Optical
5 Lithography Modeling", February 27, 2000. For large features to be exposed, there is a large overlap 105 between the windows 101 and 103, as shown in Figure 2A. Therefore, in order to expose both dense and isolated regions, the corresponding value of exposure dose and defocus must be located in the overlap region 105 between the process windows 101 and 103. For large features to be
10 exposed, it is relatively easy to select appropriate values of exposure dose and defocus that fall into the large overlap region 105, as shown in Figure 2A.

[0006] However, the overlap region 205 of process windows for exposing dense 201 and isolated 203 regions in a photoresist layer is relatively small for exposed features having a small size, as shown in Figure 2B. Region 207 of process
15 window 201 and region 209 of process window 203 outside the overlap region 205 cannot be used when exposing both dense and isolated regions. Therefore, it is difficult to select the exposure conditions which are optimum for both small dense and isolated regions because the process window overlap 205 for exposing such regions is also small.

20 BRIEF SUMMARY OF THE INVENTION

[0007] According to one aspect of the present invention, there is provided a method of making plurality of features in a first layer, comprising forming a photoresist layer over the first layer, exposing dense regions in the photoresist layer through a first mask under a first set of illumination conditions, exposing at least one isolated
25 region in the photoresist layer through a second mask different from the first mask under a second set of illumination conditions different from the first set of illumination conditions, patterning the exposed photoresist layer, and patterning the first layer using the patterned photoresist layer as a mask.

0008] According to another aspect of the present invention, there is provided a method of making a semiconductor device comprising forming a first layer of the semiconductor device, forming a photoresist layer over the first layer, exposing dense regions in the photoresist layer through a first mask using a first focus, exposing isolated regions in the photoresist layer through a second mask different from the first mask using a second focus different from the first focus, removing the exposed dense and isolated regions in the photoresist layer to form a patterned photoresist layer, and etching the first layer using the patterned photoresist layer as a mask.

0009] According to another aspect of the present invention, there is provided a method of making a semiconductor device, comprising forming at least one semiconductor device on a substrate, forming a first insulating layer over the semiconductor device, forming a photoresist layer over the first insulating layer, and exposing dense regions in the photoresist layer through a first mask using a first focus. The method further comprises exposing isolated regions in the photoresist layer through a second mask different from the first mask using a second focus different from the first focus, removing the exposed dense and isolated regions in the photoresist layer to form dense and isolated openings in the photoresist layer, providing an etching gas or an etching liquid to the first insulating layer through the dense and the isolated openings in the photoresist layer to form a plurality of dense and isolated openings in the first insulating layer, and forming a conductive material in the dense and the isolated openings.

BRIEF DESCRIPTION OF THE DRAWINGS

0010] Figures 1A, 1B and 1C are side cross sectional views of a prior art method of making vias.

0011] Figures 2A and 2B are illustrations of process windows on plots of exposure dose versus defocus values.

[0012] Figure 3 is a side cross sectional view of a photoresist layer containing dense and isolated exposed regions.

[0013] Figures 4A, 4B, 4C and 4D are side cross sectional views of a photolithography method according to a first preferred embodiment of the present invention.

[0014] Figures 5A, 5B, 5C and 5D are side cross sectional views of a photolithography method according to a second preferred embodiment of the present invention.

[0015] Figure 6 is a side cross sectional view of features made by a photolithography method according to an alternative preferred embodiment of the present invention.

[0016] Figure 7 is a partial side cross sectional view of a completed semiconductor device made by the method of the preferred embodiments of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0017] The present inventors have determined that patterning errors may be decreased if the dense photoresist regions and the isolated photoresist regions are exposed through separate masks or reticles under different illumination conditions (i.e., different optical settings). By using separate masks to expose dense and isolated photoresist regions, the illumination conditions may be optimized for the dense and the isolated photoresist regions. Furthermore, in contrast to the prior art method of exposing dense and isolated regions through the same mask, by using separate masks to expose dense and isolated regions, the available process windows for the exposure of the dense and isolated regions are not restricted to the overlap region between the dense and the isolated region process windows.

[0018] As used herein, dense exposed regions are spaced closer together than isolated exposed regions (i.e., the dense regions have a smaller pitch than the isolated regions). A different set optimum of illumination conditions provides an

optimum exposure for the dense regions and for the isolated regions. In a preferred aspect of the present invention, the term "dense regions" includes, but is not limited to, exposed regions that are within 500 nm, preferably within 300 nm of another exposed region in the photoresist layer. The term "isolated", includes but is not limited to, exposed regions that are farther than 500 nm, preferably farther than 1 micron from the nearest another exposed region in the photoresist layer. However, the exposed regions are not necessarily classified into "dense" and "isolated". For example, exposed regions that are between 301 and 999 nm away from the nearest other exposed region may be considered to be "semi-dense," and may be exposed through a third mask using a third set of illumination conditions. Furthermore, there may be several sets of semi-dense regions, depending on the application, which may be exposed through separate masks under different sets of illumination conditions than other sets of regions.

As used herein, illumination conditions include any optical setting for the exposure system (i.e., the illumination system) used to expose the photoresist layer. These conditions include any one or more of focus, partial coherence, numerical aperture width, illumination type and any other relevant setting of the exposure system which affect the size and location of the exposed regions. Focus refers to the distance between the photolithographic mask (i.e. mask or reticle) and the lens of the exposure system. Partial coherence (σ) is a function of the intensity of radiation that reaches the mask (i.e. mask or reticle). Illumination type includes conventional illumination or annular illumination that is used to expose the photoresist layer. The specific illumination conditions are dependent on the particular type of exposure system, width of the mask openings, the desired pattern to be exposed in the photoresist pattern and other factors. The illumination conditions may be optimized by using a simulation program that is used with the exposure system.

The values of exposure dose and defocus used to expose the dense and/or the isolated regions are not restricted to values in the process window overlap. With reference to Figure 2B, the values of exposure dose and defocus used to expose the

09887035-062501

dense regions through a first mask may be located in region 207 of the dense region process window 201 which is outside the overlap region 205. The values of exposure dose and defocus used to expose the isolated regions through a second mask may be different than those used to expose the dense regions. The values of exposure dose and defocus used to expose the isolated regions may be located in region 209 of the isolated region process window 203 which is outside the overlap region 205. Thus, with reference to Figure 2B, if desired, the values of exposure dose and defocus used to expose the dense regions and/or the isolated regions may be located in region 207 and/or 209 of a respective process window 201, 203 outside the overlap region 205 between the respective process windows 201, 203. Of course, the values of the exposure dose and defocus for dense and/or isolated regions may be located in the overlap region 205, if desired. Therefore, by using separate masks to expose dense and isolated regions, the process windows are expanded.

Figure 3 illustrates an example of dense and isolated exposed regions. In Figure 3, a photoresist layer 3 is formed over a first layer 1, such as a semiconductor, insulating or conductive layer. The photoresist layer 3, may be a positive or a negative photoresist layer, as will be explained in more detail below. A plurality of exposed regions 5A, 5B, 5C, 7A and 7B are present in the photoresist layer 3. Dense regions 5A, 5B and 5C have a smaller pitch (i.e., distance to the nearest other exposed region) than isolated regions 7A and 7B. There may be two or more dense regions and one or more isolated regions.

Figures 4A-4D illustrate a photolithography method using a positive photoresist and two masks to form vias according to a first preferred embodiment of the present invention. A positive photoresist layer 23 is formed over the first layer 21. The photoresist layer 23 is then exposed to radiation, such as actinic light or other suitable UV radiation, through openings 31A, 31B and 31C in a first mask or reticle 29 to form a set of dense exposed regions 25A, 25B, 25C in the photoresist layer 23, as illustrated in Figure 4A. The dense exposed regions are exposed under a first set of illumination conditions, which include a first focus, partial coherence,

numerical aperture width and/or illumination type. The selected first set of illumination conditions is optimized to expose dense regions in the photoresist layer. The exposed regions 25A, 25B, 25C of the photoresist layer 23 are rendered soluble to developer. Other regions of the photoresist layer 23 are shielded by the opaque layer 34 of the mask 29 and are not exposed.

10023] The photoresist layer 23 is then exposed to radiation through openings 33A and 33B in a second mask or reticle 30, different from the first mask 29, to form isolated exposed regions 27A and 27B in the photoresist layer 23, as illustrated in Figure 4B. The isolated exposed regions are exposed under a second set of illumination conditions, which is different from the first set of illumination conditions. The selected second set of illumination conditions is optimized to expose isolated regions in the photoresist layer. Preferably the first focus used to expose the dense exposed regions differs from the second focus used to expose the isolated regions. For example, the first focus may differ from the second focus by 1 to 30%, preferably by 15-25%. However, the second partial coherence, numerical aperture width and/or illumination type may be different from the first partial coherence, numerical aperture width and/or illumination type instead of or in addition to the focus difference. The dense regions 25A, 25B and 25C are not exposed because they are shielded by an opaque region 36 of the second mask 30.

20 The exposed photoresist regions 25A, 25B, 25C, 27A, 27B are separated by non-exposed regions 26, which remain insoluble to the developer.

10024] After exposing the dense and isolated regions, the photoresist layer 23 is developed (i.e., exposed to a developer fluid) to remove the exposed, soluble photoresist from regions 25A, 25B, 25C, 27A, 27B to provide openings to layer 21, as shown in Figure 4C. Unexposed photoresist regions 26 are not removed during development, and are used as a mask for subsequent etching of layer 21. It should be noted that the order of steps may be reversed and the isolated regions may be exposed before rather than after the dense regions.

5

10

25

aperture width and/or illumination type may be different from the first second partial coherence, numerical aperture width and/or illumination type instead of or in addition to the focus difference. The exposure to radiation crosslinks the photoresist in regions 47A, 47B, rendering these regions insoluble to developer. The exposed photoresist regions 45A, 45B, 45C, 47A, 47B are separated by the non-exposed regions 46A, 46B, 48A, and 48B which are shielded by the opaque layer 56 of the second mask 50.

[0028] After exposing the dense and isolated regions 45A, 45B, 45C, 47A, 47B, the photoresist layer 43 is developed to remove the uncrosslinked photoresist from the unexposed regions 46A, 46B, 48A, and 48B to provide openings to layer 41, as shown in Figure 5C. Photoresist regions 45A, 45B, 45C, 47A, 47B are not removed during development and are used as a mask for subsequent etching of layer 41. If desired, the order of steps of Figures 5A and 5B may be reversed, and regions 47A, 47B may be exposed through the second mask 50 before regions 45A, 45B, 45C are exposed through the first mask 49.

[0029] After the openings are provided in the photoresist layer 43, the openings or vias 55 are formed in layer 41 by providing an etching gas or an etching liquid to the first layer through the openings in the photoresist layer 43. Thus, vias 55 separated by intervias 59 are formed in layer 41, as illustrated in Figure 5D.

[0030] While Figures 4A-4D and 5A-5D illustrate only five and four vias respectively, for ease of explanation, it should be understood that a semiconductor device may contain any number of a plurality of vias. Furthermore, the photolithography method of the preferred embodiments is not limited to forming vias in an insulating layer. The photoresist layer containing dense and isolated exposed regions, after being developed, may be used to as a mask to pattern an underlying semiconductor or a conductive layer. For example, an etching gas or an etching liquid may be provided to the conductive or semiconductor layer through openings in the patterned photoresist layer to form a plurality of features in this layer. Thus, conductive interconnects or electrodes, such as gate electrodes, or

semiconductor mesas, such as emitter regions of a bipolar transistor, may be patterned according to the preferred embodiments of the present invention. Figure 6 illustrates an exemplary, in-process semiconductor device, where dense metal electrodes 57A, 57B, 57C are patterned after exposed dense 25A, 25B and isolated 5 27A regions of a positive photoresist layer 23 are developed and removed.

10031] Figure 7 illustrates a completed semiconductor device 60 containing the vias made by the methods of the first or second preferred embodiment. The semiconductor device 60 contains a substrate 61, which may be a semiconductor (such as silicon or gallium arsenide, etc.), a glass or a plastic material. One or 10 more active elements 63 are formed on the substrate 61. The active element may comprise at least one of a MOSFET, a MESFET, a bipolar transistor, a capacitor, a resistor or any other desired device. For example, Figure 7 illustrates a MOSFET 63.

10032] The MOSFET 63 contains doped source and drain regions 65 in the substrate 15 61, a gate electrode 67 with sidewall spacers and a gate dielectric 69 between the gate electrode and the channel region in the substrate 61. At least one insulating layer overlies the active element 63. For example, the at least one insulating layer includes a first level insulating layer 71 and a first intermetal dielectric 73, as illustrated in Figure 7. It should be understood that there may be other plural 20 intermetal dielectric layers above layer 73 that contain vias. The insulating layers 71, 73 may comprise any dielectric layer, such as at least one of silicon oxide, silicon nitride, silicon oxynitride, fluorinated silicon oxide, aluminum oxide, tantalum oxide, BPSG, PSG, BSG or spin on glass. In should be noted that the insulating layers 71, 73 may comprise plural sublayers of different dielectric 25 materials, if desired.

10033] The first level intermetal dielectric layer 73 contains dense vias 75A, 75B and isolated via 77A. The vias are formed using two masks, as illustrated in Figures 4A-4D or 5A-5D. For example, vias 75A, 75B, may be formed using mask 29 and via 77A, may be formed using mask 30. Conductive first level interconnect

metallization layers 79 are formed in the vias. The metallization layers 79 may extend to the electrodes 80 of the active device 63, such that the metallization layers 79 contact the electrodes 80. The metallization 79 material may be selected from at least one of polysilicon, aluminum, copper, tungsten, titanium, titanium nitride or metal silicide. A second level intermetal dielectric layer 81 overlies metallization layers 79. If desired, the metallization 79 may also be formed using two masks, as described in reference to Figure 6.

[0034] While the invention has been described in detail and with reference to specific embodiments thereof, it will be apparent to one skilled in the art that various changes and modifications can be made therein without departing from the scope of the invention. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.